Claims

[c1] 1. A method for fetching at least one word instruction from a memory in a word-based processor, wherein the word instruction includes types of a full-word instruction or a half-word instruction, the processor employs a data bus with a word length in bit, the method comprising:
dividing the word length into a plurality of world units, wherein each of the word units has a size of 2^n bits;
checking a memory request to know whether or not the word instruction to be fetched is in a first type address or a second type address, wherein the first type address is a sequential half-word non-aligned address and the second type address is other than the first type address;
fetching the word instruction at each of fetch cycles, if the second type address is a current status;
fetching the sequential half-word instruction simultaneously in the full word length at a first fetch cycle, if the word instruction is at the first type address, wherein the half-word instructions are stored in the word units; and
executing the half-word instructions without directly fetching the half-word instructions from the memory in next fetch cycles to the first fetch cycle.

[c2] 2. The method of claim 1, wherein the second type address comprises a word aligned address and a non-sequential address.

[c3] 3. The method of claim 2, wherein the non-sequential address is an address not following a previous address by one word unit.

[c4] 4. The method of claim 1, wherein the sequential half-word non-aligned address is an address following a previous address by one word unit.

[c5] 5. The method of claim 1, wherein the size of the word unit is 8 bits, 16 bits or 32 bits.

[c6] 6. The method of claim 1, wherein the full world instruction has a size of 64 bits and the half-word instruction has a size of 32 bits.

[c7] 7. The method of claim 1, wherein the step of executing the half-word instructions comprises obtaining instruction addresses with respect to the half-

word instructions and getting contents of the half-word instructions.

[c8] 8. A circuit structure suitable for fetching word instructions in a word-based processor, which employs a data bus with a word length in bits, the circuit comprising:
a multiplexer;
a flip-flop unit; and
an OR logic gate,
wherein the multiplexer has a first input terminal for receiving a memory data of the word instructions in the full word length and a second input terminal for receiving a recirculated portion of the word length feedback from an output of the flip-flop unit,
wherein the OR logic gate receives a word-aligned signal and a non-sequential signal, and exports a selection signal to the multiplexer to select data from one of the first and second input terminals,
wherein the output of the multiplexer is input to the flip-flip unit, and the flip-flip unit exports a desired instruction and the recirculated portion of the word length is fed back to the multiplexer,
whereby when the recirculated portion of the word length is selected at the multiplexer, the processor is not necessary to actually fetch the memory data.

[c9] 9. The circuit of claim 8, wherein the recirculated portion of the word length has a size of 2^{n} bits.

[c10] 10. The circuit of claim 9, wherein the size of the recirculated portion of the word length includes 8 bits, 16 bits, or 32 bits.

[c11] 11. The circuit of claim 8, wherein the non-sequential signal is an address not following a previous address by a size of the recirculated portion of the word length.

[c12] 12. The circuit of claim 8, wherein when the output of the OR logic gate is a false state, it indicates that the word instruction is a type of sequential half-word instructions.

[c13] 13. A circuit structure suitable for fetching word instructions in a word-based

processor, which employs a data bus with a word length in bits, wherein the word length can be divided into a plurality of word units with a size of 2^n bits, the circuit comprising:

a multiplexer;

a flip-flop unit; and

an OR logic gate,

wherein the multiplexer has a first input terminal for receiving a memory data of the word instructions in the full word length, and a second input terminal for receiving a portion of the word length in the word units feedback from an output of the flip-flop unit,

wherein the OR logic gate receives a word-aligned signal and a non-sequential signal, and exports a selection signal to the multiplexer to select data from one of the first and second input terminals,

wherein the output of the multiplexer is input to the flip-flip unit, and the flip-flip unit exports a desired instruction and a portion of the word length not being used is fed back to the multiplexer,

whereby when the recirculated portion of the word length is selected at the multiplexer, the processor is not necessary to actually fetch the memory data.

[c14] 14. The circuit of claim 13, wherein the recirculated portion of the word length has a size of 8 bits, 16 bits, or 32 bits.

[c15] 15. The circuit of claim 13, wherein the non-sequential signal is an address not following a previous address by a size of the recirculated portion of the word length.

[c16] 16. The circuit of claim 13, wherein when the output of the OR logic gate is a false state, it indicates that the word instruction is a type of sequential half-word instructions.